

Appn Number: 10/010,132Docket Number: MS-01CXT0161M**IN THE CLAIMS:**

1-4. (Canceled)

5. (Currently Amended): A computer system, comprising:

a plurality of point-to-point interface units comprising a computer module interface and a point-to-point interface;

a plurality of computer modules connected to the computer module interface of the plurality of point-to-point interface units; and

at least one bus emulator connected to the point-to-point interface of the plurality of point-to-point interface units, wherein the at least one bus emulator is capable of supporting only one transfer at a time, the at least one bus emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase a fan-out of the at least one bus emulator, thereby increasing a signal length accommodated by the at least one bus emulator.

6. (Currently Amended) The computer system of claim 5, wherein the plurality of point-to-point interface units each comprise a parallel-to-serial conversion unit units that operate upon detecting that detects the beginning of a data transfer cycle presented to the computer module interface and wherein the parallel-to-serial conversion units that accept accept a data field, and an address field and a cycle-type indicator from the computer module interface.

7. (Original) The computer system of claim 5 wherein the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

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8. (Currently Amended) The computer system of claim 5 wherein the at least one bus emulator comprises: a plurality of point-to-point interfaces interconnected by an internal bus.

9. (Original) The computer system of claim 8 further comprising an arbiter for granting access to the internal bus to one of the plurality of point-to-point interfaces.

10. (Cancelled)

11. (Currently Amended) A computer module, comprising:  
a point-to-point interface capable of interacting with a at least one bus emulator that is capable of supporting one bus transfer at a time; and  
the at least one bus emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase a fan-out of the at least one bus emulator, thereby increasing a signal length accommodated by the at least one bus emulator.

12. (Currently Amended) The computer module of claim 11 wherein the point-to-point interface comprises:

a parallel-to-serial conversion unit that operates upon detecting the beginning of a data transfer cycle presented to the computer module interface; and  
wherein the parallel-to-serial conversion units accept a data field and an address field and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface.

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13. (Original) The computer module of claim 11 wherein the point-to-point interface comprises high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

14. (Currently Amended) A point-to-point interface unit, comprising:  
a computer module interface and a point-to-point interface, wherein the point-to-point interface is capable of interacting with a at least one bus emulator that is capable of supporting one bus transfer at a time; and  
the at least one bus emulator having a cascade port providing an ability to couple a plurality of bus emulators in a daisy chain to increase a fan-out of the at least one bus emulator, thereby increasing a signal length accommodated by the at least one bus emulator.

15. (Currently Amended) The point-to-point interface unit of claim 14, further comprising:  
a parallel-to-serial conversion unit that operates operate upon detecting the beginning of a data transfer cycle presented to the computer module interface; and wherein the parallel-to-serial conversion units accept a data field, and an address field, and a cycle-type indicator from the computer module interface and delivers a serial output comprising a data transfer cycle to the point-to-point interface.

16. (Original) The computer system of claim 14 wherein the plurality of point-to-point interface units comprise high-current parallel drivers capable of propagating data, address and data transfer cycle requests.

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17. (Currently Amended): A bus emulator comprising:  
at least one internal bus capable of supporting one bus transfer at a time;  
and  
a plurality of point-to-point interfaces interconnected by the internal bus;  
and  
a cascade port providing an ability to couple a plurality of bus emulators in  
a daisy chain to increase a fan-out of the at least one bus emulator, thereby increasing  
a signal length accommodated by the at least one bus emulator.

18. (Currently Amended): The bus emulator of claim 17 further comprising an arbiter for granting access to the at least one internal bus to one of the plurality of point-to-point interfaces.

19. (Cancelled)